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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/620,057 | 07/15/2003 | Aritharan Thurairajaratnam | 02-4456/1P | 7679 |

24319 7590 01/14/2005

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| EXAMINER | |
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| CHAN, EMILY Y | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2829 | |

DATE MAILED: 01/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/620,057 | THURAIRAJARATNAM ET AL. | |
| | Examiner | Art Unit | |
| | Emily Y Chan | 2829 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *07 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-10,14 -23 and 27* is/are pending in the application.

4a) Of the above claim(s) *11-13 and 24-26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10, 14 -23 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In claim 1, the added "means configured to use the data to calculate interconnect impedance versus time data for the DUT" is not described in the specification and shown in the drawings.

### *Specification*

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1,10, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Graude, U S. Patent No. 4, 739,276 (Graube '276) in view of Goto Nobumasa et al ('2002-148291).

Graube ('276) discloses a method and apparatus (see Figs 2-3) for measuring the impedance signature of a network or a connecting cable (see Col. 1, lines 65-66) as claimed, comprising:

A tester (computer 20),

A device under test (12,14,16),

The tester (computer 20) being connected to a Digital Sample Oscilloscope (10) and the Digital Sample Oscilloscope (10) configured to launch a signal (34,36) received by the device under test (12,14,16) (see Col. 4, lines 27-33) and configured to receive a reflected signal (see Col. 5, lines 19-23) from the device under test (12, 14, 16),

The tester (computer 20) configured to obtain a waveform (see Fig 3) from the Digital Sample Oscilloscope (10) and store data in a file (see Col. 4, lines 50-55), and

Means (computer 20) configured to use the data to "calculate" interconnect impedance versus time data for the device under test (12, 14,16) (see Col. 5, lines 40-42).

Graube ('276) further teach using post processing software (see Col. 5, line 41 "simple algorithm") to analyze the data and provide interconnect impedance versus time data.

Graube ('276) does not specify that his device under test (12,14,16) is a load board configured to retain a substrate and the signal (34,36) which is launched by the Digital Sample Oscilloscope (10) is received by the substrate.

Goto Nobumasa et al ('2002-148291) disclose a measuring instrument (Fig. 1) for characteristic impedance and particularly teach that a device under test is a printed wiring board 5 configured to retain a substrate (51, 52) and a Digital Sampling Oscilloscope (TDR meter 2) which is configured to launch a signal received by the substrate (DUT 5) (see SOLUTION "TDR meter 2 sends an electrical signal to a printed wiring board 5 ").

It would have been obvious to one of ordinary skilled in the art at the time the invention was made to incorporate the feature of using the TDR for sending the signal to the substrate of device under test as taught by Goto Nobumasa et al ('2002-148291) into Graube ('276) 's method and apparatus so that Graube ('276) 's system is capable of performing an impedance measurement wherein the device under test retains a substrate as claimed because Goto Nobumasa et al ('2002-148291) clearly disclose that their impedance measuring instrument can efficiently take a measurement (see abstract: PROBLEM TO BE SOLVED).

3. Claims 2-6, 8,16-20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Graube ('276) in view of Goto Nobumasa et al ('2002-148291) as applied to claim1, 10,14- 15 and 27 above, and further in view of Hembree et al, U S Patent No. 6,218,848 (Hembree et al '848).

With claims 2-6 and 16-20, Graube ('276) in view of Goto Nobumasa et al ('2002-148291) do not specify a probe card mounted to the tester and the tester includes a test head.

Hembree et al ('848) disclose a semiconductor probe card having resistance measuring circuitry (see Fig 3) and a method for measuring package interconnect impedance (resistivity contact) (see Col. 2, lines 53-56) as claimed, comprising:
a tester (26) which includes a test head (30) for obtaining a waveform and storing a data in a file (see Col. 7, lines 52-55), and a probe card (20) mounted to the tester (26) for contacting a substrate of device under test (12) (see Col 4, line 15) and having probe pins (22). Furthermore, Hembree et al ('848) teach that their probe pins (22) from the

probe card (20) make contact with bump pads (44) on the substrate (see Col. 6, lines 17-23).

It would have been obvious to one of skilled in the art at the time the claimed invention was made to incorporate the teaching of Hembree et al ('848) into Graube ('276) in view of Goto Nobumasa et al ('2002-148291) 's system for the expected benefit of providing a improved probe card that includes resisitivity measuring circuit for testing semiconductor device as disclosed by Hembree et al ('848) (see Col. 1, line12, and Col. 2, lines 31-33).

With claims 8 and 22, Goto Nobumasa et al ('2002-148291) teach a coaxial cable (3) that connects the TDR (2) to a test head (probe 4).

4 Claims 7 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Graube ('276) in view of Goto Nobumasa et al ('2002-148291) as applied to claims 1 and 15 respectively above, and further in view of Shahriari et al, U S Patent No. 6,535,006 (Shahriari et al '006).

Graube ('276) in view of Goto Nobumasa et al ('2002-148291) do not disclose a socket, which is configured to hold the substrate for test.

Shahriari et al ('006) disclose a test socket system (see Fig 1a) and particularly teach a socket (106) wherein a package electronic circuit is mounted in a socket (106) for testing (see Col. 2, lines 47-48).

It would have been obvious to one of ordinary skilled in the art to incorporate the teaching of Shahriari et al ('006) 's socket (106) into Graube ('276) and Goto Nobumasa et al ('2002-148291)' s system so that a test socket is used to hold the substrate for test

in order to provide more accuracy testing of electrical characteristics as disclosed by Shahriari et al ('006) (see Col.1 BACKGROUND).

5. Claims 9 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Graube ('276) in view of in view of Goto Nobumasa et al ('2002-148291) as applied to claims 1 and 15 respectively above, and further in view of Ayadi, 2003-0078748 (Ayadi '748).

Graube ('276) in view of in view of Goto Nobumasa et al ('2002-148291) do not teach a GPIB cable that connects the TDR to the tester.

Ayadi ('748) discloses a graphical user interface for testing integrated circuit (see Fig. 1) and particularly teach a coaxial cable (21) (see page 2, paragraph 0026, line 2) which connects the DSO (test instrument 13) to the probe card (20) and a GPIB cable (22) (see page 3, paragraph 0041, line 6-8) which connects the DSO (test instrument 13) to the tester (computer 23).

It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Ayadi ('748) 's coaxial and GPIB cables into Graube ('276) and Goto Nobumasa et al ('2002-148291)' s system so to ensure the communication between the test instruments and the tester or computer as disclosed by Ayadi ('748) (see page 3, paragraph 0042, lines 9-10).

***Response to Arguments***

Applicant's arguments with respect to claims 1and 15 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emily Y Chan whose telephone number is 571-272-1956. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on 571-272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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DAVID ZARNEKE
PRIMARY EXAMINER
1/10/05